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EXAMINER	
LI, AIMEE J	

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2183	

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Pepper Hamilton LLP
50th Floor
One Mellon Center
500 Grant Street
Pittsburgh, PA 15219

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,186	KLEIN, ROBERT C.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☒ Claim(s) *17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/23/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-26 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Specification, Drawings, Abstract, Claims, Oath and Declaration, and IDS as received on 23 July 2003.

Claim Objections

3. Claim 17 is objected to because of the following informalities: Please correct "determining the routing or one or more multiplexers within the processing element" to read -- determining the routing [[or]]of one or more multiplexers within the processing element--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-26 are rejected under 35 U.S.C. 102(b) as being taught by Horst, U.S. Patent Number 5,404,550 (herein referred to as Horst).

6. Referring to claim 1, Horst has taught a processing element, comprising:

   a. A system bus interface (Horst column 2, line 61 to column 3, line 5 and Figure 1);

   b. An instruction handler (Horst column 4, line 1 to column 5, line 2 and Figure 5);

c. An input router and conditioner electrically connected to the system bus interface and the instruction handler (Horst column 4, line 1 to column 5, line 2 and Figure 5);

d. An ALU electrically connected to the input router and conditioner (Horst column 4, line 1 to column 5, line 2 and Figure 5);

e. A memory electrically connected to the input router and conditioner (Horst column 4, line 1 to column 5, line 2 and Figure 5); and

f. An output router electrically connected to the ALU, the memory and the input router and conditioner (Horst column 4, line 1 to column 5, line 2 and Figure 5).

7. Referring to claim 2, Horst has taught wherein the system bus interface and instruction handler comprise:

a. A connection to a system bus, wherein the system bus comprises a plurality of address lines and a plurality of data lines (Horst column 3, lines 33-66; column 4, line 1 to column 5, line 2; Figure 3; Figure 4; and Figure 5);

b. An address decoder, electrically connected to one or more of the plurality of address lines, for determining whether the processing element is selected by comparing a value contained on the one or more address lines with a decoding value and asserting an enable flag when the processing element is selected (Horst column 4, line 1 to column 5, line 2 and Figure 5). In regards to Horst, the output from the comparator to the receiving queue is the flag, since that is how the processing element receives the packet in order to know that it is the destined element.

c. An instruction register, electrically connected to one or more of the plurality of address lines and one or more of the plurality of data lines, for storing the values contained on the one or more address lines and the one or more data lines when the enable flag is asserted (Horst column 4, line 1 to column 5, line 2 and Figure 5); and

d. A state machine, electrically connected to the instruction register, for configuring the processing element based on at least one of the stored address value and the stored data value (Horst column 3, lines 33-66; column 4, line 1 to column 5, line 2; Figure 3; Figure 4; and Figure 5). In regards to Horst, a state machine is inherent to determine the proper operation of the device. Please see Heuring and Jordan's Computer Systems Design and Architecture pages 525-534.

8. Referring to claims 3 and 10, taking 10 as exemplary, Horst has taught wherein the input router and conditioner comprises:

a. A first input path electrically connected to an output of a first input processing element (Horst column 5, lines 19-43 and Figure 6);

b. A second input path electrically connected to all output of a second input processing element (Horst column 5, lines 19-43 and Figure 6);

c. A third input path electrically connected to an output of a third input processing element (Horst column 5, lines 19-43 and Figure 6);

d. One or more multiplexers for determining a data value, an address/data value, and a carry bit (Horst column 4, line 1 to column 5, line 2; column 8, lines 25-31; and Figure 5). In regards to Horst, it is understood that when a multiplication is

broken into multiple ADD operations, the carry bit is part of the operations. Please see Heuring and Jordan's Computer Systems and Design Architecture pages 270-276 for more information.

e. Circuitry for selectively performing one or more operations on at least one of the data value and the address/data value and the carry bit (Horst column 4, line 1 to column 5, line 2; column 8, lines 25-31; and Figure 5);

f. Wherein the one or more operations include:

i. Performing a bit shift operation on at least one of the data value and the address/data value (Horst column 6, lines 1-9 and Figure 7),

ii. Incrementing at least one of the data value and the address/data value (Horst column 6, lines 1-9 and Figure 7),

iii. Decrementing at least one of the data value and the address/data value (Horst column 6, lines 1-9 and Figure 7),

iv. Storing at least one of the data value and the address/data value (Horst column 6, lines 1-9 and Figure 7), and

v. Passing through at least one of the data value and the address/data value (Horst column 4, line 1 to column 5, line 2; column 10, line 41 to column 11, line 5; and Figure 5).

9. Claim 3 is similar in limitation to claim 10 and is rejected for the same reasons as claim 10 set forth above. Claim 3 differs only in that it does not explicitly state performing operations on the carry bit.

10. Referring to claim 4, Horst has taught wherein the input router and conditioner further comprises a fourth input path electrically connected to a feedback path (Horst column 4, line 1 to column 5, line 2; column 5, lines 19-43; Figure 5; and Figure 6).

11. Referring to claim 5, Horst has taught wherein the input router and conditioner further comprises a fourth input path electrically connected to a system bus (Horst column 4, line 1 to column 5, line 2 and Figure 5).

12. Referring to claims 6 and 11, taking claim 11 as exemplary, Horst has taught wherein the one or more multiplexers comprise:

a. A first multiplexer for determining a first portion of the data value (Horst column 4, line 1 to column 5, line 2; column 10, line 41 to column 11, line 5; and Figure 5);

b. A second multiplexer for determining a second portion of the data value (Horst column 4, line 1 to column 5, line 2; column 10, line 41 to column 11, line 5; and Figure 5);

c. A third multiplexer for determining a first portion of the address/data value (Horst column 4, line 1 to column 5, line 2; column 10, line 41 to column 11, line 5; and Figure 5); and

d. A fourth multiplexer for determining a second portion of the address/data value (Horst column 4, line 1 to column 5, line 2; column 10, line 41 to column 11, line 5; and Figure 5); and

e. A fifth multiplexer for determining the carry bit (Horst column 4, line 1 to column 5, line 2; column 5, lines 19-43; column 10, line 41 to column 11, line 5; and Figure 5).

13. Claim 6 is similar in limitation to claim 11 and is rejected for the same reasons as claim 10 set forth above. Claim 6 differs only in that it does not explicitly state performing operations on the carry bit.

14. Referring to claim 7, Horst has taught wherein the first portion of the data value and the second portion of the data value are of equal width (Horst column 4, line 1 to column 5, line 2; column 10, line 41 to column 11, line 5; and Figure 5).

15. Referring to claim 8, Horst has taught wherein the first portion of the address/data value and the second portion of the address/data value are of equal width (Horst column 4, line 1 to column 5, line 2; column 10, line 41 to column 11, line 5; and Figure 5).

16. Referring to claim 9, Horst has taught wherein the first input processing element is located along an x-axis with reference to the processing element, the second input processing element is located along a y-axis with reference to the processing element, and the third input processing element is located in a diagonal direction with reference to the processing element (Horst column 5, lines 19-43 and Figure 6).

17. Referring to claim 12, Horst has taught wherein the output router comprises:

a. A first input path electrically connected to an output of a first input processing element (Horst column 5, lines 19-43 and Figure 6);

b. A second input path electrically connected to all output of a second input processing element (Horst column 5, lines 19-43 and Figure 6);

c. A third input path electrically connected to an output of a third input processing element (Horst column 5, lines 19-43 and Figure 6).

18. Referring to claim 13, Horst has taught wherein the output router further comprises a fourth output path electrically connected to a feedback path (Horst column 4, line 1 to column 5, line 2; column 5, lines 19-43; Figure 5; and Figure 6).

19. Referring to claim 14, Horst has taught wherein the output router further comprises a fourth output path electrically connected to a system data bus (Horst column 4, line 1 to column 5, line 2 and Figure 5).

20. Referring to claim 15, Horst has taught wherein the first output processing element is located along an x-axis with reference to the processing element, the second output processing element is located along a y-axis with reference to the processing element, and the third output processing element is located in a diagonal direction with reference to the processing element (Horst column 5, lines 19-43 and Figure 6).

21. Referring to claims 16 and 19, taking claim 16 as exemplary, Horst has taught a method of configuring a processing element comprising:

a. Providing an address value and a data value to the processing element (Horst column 3, lines 33-66; column 4, line 1 to column 5, line 2; Figure 3; Figure 4; and Figure 5);

b. Decoding the address value (Horst column 4, line 1 to column 5, line 2 and Figure 5);

c. Determining from the decoded address value whether the processing element is selected (Horst column 4, line 1 to column 5, line 2 and Figure 5);

d. If the processing element is selected, storing at least a portion of the address value and the data value (Horst column 3, lines 33-66; column 4, line 1 to column 5, line 2; Figure 3; Figure 4; and Figure 5);

e. Loading the stored address value and the stored data value into a state machine associated with the processing element (Horst column 3, lines 33-66; column 4, line 1 to column 5, line 2; Figure 3; Figure 4; and Figure 5); and

f. Configuring, by the state machine, the processing element based on the stored address value and the stored data value (Horst column 3, lines 33-66; column 4, line 1 to column 5, line 2; Figure 3; Figure 4; and Figure 5). In regards to Horst, a state machine is inherent to determine the proper operation of the device. Please see Heuring and Jordan's Computer Systems Design and Architecture pages 525-534.

22. Claim 19 is similar in limitation to claim 16 and is rejected for the same reasons as claim 10 set forth above. Claim 16 differs only in that it does not explicitly state providing and using a data value.

23. Referring to claim 17, Horst has taught wherein the configuring step comprises:

a. Enabling one or more components of the processing element (Horst column 3, lines 33-66; column 4, line 1 to column 5, line 2; Figure 3; Figure 4; and Figure 5); and

b. Determining the routing of one or more multiplexers within the processing element (Horst column 4, line 1 to column 5, line 2; column 8, lines 25-31; and Figure 5).

24. Referring to claim 18, Horst has taught wherein the configuring step further comprises storing one or more values, determined by at least one of the stored address value and the stored data value, in a memory (Horst column 6, lines 1-9 and Figure 7).

25. .Referring to claim 20, Horst has taught a processing element, comprising:

a. An input block (Horst column 4, line 1 to column 5, line 2 and Figure 5); and

b. An output block (Horst column 4, line 1 to column 5, line 2 and Figure 5),

c. Wherein the input block comprises:

i. A first input path electrically connected to an output of a first input processing element (Horst column 5, lines 19-43 and Figure 6),

ii. A second input path electrically connected to an output of a second input processing element (Horst column 5, lines 19-43 and Figure 6),

iii. A third input path electrically connected to an output of a third input processing element (Horst column 5, lines 19-43 and Figure 6), and

d. Wherein the output block comprises:

i. A first output path electrically connected to an input of a first output processing element (Horst column 5, lines 19-43 and Figure 6),

ii. A second output path electrically connected to an input of a second output processing element (Horst column 5, lines 19-43 and Figure 6), and

iii. A third output path electrically connected to an input of a third output processing element (Horst column 5, lines 19-43 and Figure 6).

26. Referring to claim 21, Horst has taught wherein the input block further comprises a fourth input path electrically connected to a feedback path (Horst column 4, line 1 to column 5, line 2; column 5, lines 19-43; Figure 5; and Figure 6).

27. Referring to claim 22, Horst has taught wherein the input block further comprises a fourth input path electrically connected to a system bus (Horst column 4, line 1 to column 5, line 2 and Figure 5).

28. Referring to claim 23, Horst has taught wherein the first input processing element is located along an x-axis with reference to the processing element, the second input processing element is located along a y-axis with reference to the processing element, and the third input processing element is located in a diagonal direction with reference to the processing element (Horst column 5, lines 19-43 and Figure 6).

29. Referring to claims 24, Horst has taught wherein the output block further comprises a fourth output path electrically connected to a feedback path (Horst column 4, line 1 to column 5, line 2; column 5, lines 19-43; Figure 5; and Figure 6).

30. Referring to claim 25, Horst has taught wherein the output block further comprises a fourth output path electrically connected to a system bus (Horst column 4, line 1 to column 5, line 2 and Figure 5).

31. Referring to claim 26, Horst has taught wherein the first output processing element is located along an x-axis with reference to the processing element, the second output processing element is located along a y-axis with reference to the processing element, and the third output processing element is located in a diagonal direction with reference to the processing element (Horst column 5, lines 19-43 and Figure 6).

Conclusion

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Martin, U.S. Patent Number 4,466,064, has taught an array processing system.

b. Mattheyses et al., U.S. Patent Number 4,910,665, has taught an array processor with multiplexers and shifters.

c. Dawes, U.S. Patent Number 4,967,340, has taught an array processor with multiple states for the interconnectors.

d. Dahl, U.S. Patent Number 5,247,694, has taught an array processor with input and output routers.

e. Nakagoshi et al., U.S. Patent Number 5,377,333, has taught an array processor with switch interconnections.

f. Gove et al., U.S. Patent Number 5,613,146, has taught an array processor with connections networks and configurable execution units.

g. Park et al., U.S. Patent Number 6,680,915, has taught an array processor with routers.

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

34. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

35. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
17 March 2006

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100